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\* Design Summary \*

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Top Level Output File Name : sign\_extend.ngc

Primitive and Black Box Usage:

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# FlipFlops/Latches : 32

# FD : 32

# Clock Buffers : 1

# BUFGP : 1

# IO Buffers : 48

# IBUF : 16

# OBUF : 32

Device utilization summary:

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Selected Device : 6slx9tqg144-3

Slice Logic Utilization:

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 0

Number with an unused Flip Flop: 0 out of 0

Number with an unused LUT: 0 out of 0

Number of fully used LUT-FF pairs: 0 out of 0

Number of unique control sets: 1

IO Utilization:

Number of IOs: 49

Number of bonded IOBs: 49 out of 102 48%

IOB Flip Flops/Latches: 32

Specific Feature Utilization:

Number of BUFG/BUFGCTRLs: 1 out of 16 6%

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Partition Resource Summary:

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No Partitions were found in this design.

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Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

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Clock Signal | Clock buffer(FF name) | Load |

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clk | BUFGP | 32 |

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Asynchronous Control Signals Information:

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No asynchronous control signals found in this design

Timing Summary:

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Speed Grade: -3

Minimum period: No path found

Minimum input arrival time before clock: 2.351ns

Maximum output required time after clock: 3.597ns

Maximum combinational path delay: No path found

Timing Details:

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All values displayed in nanoseconds (ns)

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Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'

Total number of paths / destination ports: 32 / 32

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Offset: 2.351ns (Levels of Logic = 1)

Source: in<15> (PAD)

Destination: in\_extend\_15 (FF)

Destination Clock: clk rising

Data Path: in<15> to in\_extend\_15

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

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IBUF:I->O 17 1.222 1.027 in\_15\_IBUF (in\_15\_IBUF)

FD:D 0.102 in\_extend\_15

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Total 2.351ns (1.324ns logic, 1.027ns route)

(56.3% logic, 43.7% route)

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Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'

Total number of paths / destination ports: 32 / 32

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Offset: 3.597ns (Levels of Logic = 1)

Source: in\_extend\_15\_1 (FF)

Destination: in\_extend<31> (PAD)

Source Clock: clk rising

Data Path: in\_extend\_15\_1 to in\_extend<31>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

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FD:C->Q 1 0.447 0.579 in\_extend\_15\_1 (in\_extend\_15\_1)

OBUF:I->O 2.571 in\_extend\_31\_OBUF (in\_extend<31>)

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Total 3.597ns (3.018ns logic, 0.579ns route)

(83.9% logic, 16.1% route)

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Cross Clock Domains Report:

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Total REAL time to Xst completion: 4.00 secs

Total CPU time to Xst completion: 4.02 secs

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Total memory usage is 4506952 kilobytes

Number of errors : 0 ( 0 filtered)

Number of warnings : 0 ( 0 filtered)

Number of infos : 1 ( 0 filtered)